6-7 ADC PCB

The ADC board, located in the PC unit is used to receive the red, green and blue analogue signals from the analysis electronics in the optical assembly, digitise them and pass them through a gradation look-up table (LUT) prior to the RISC transputer system. It also buffers the SCSI input from the host computer/OEM system.

The balance and black clamp adjustments, used to match the three analogue channels in the Analysis Optical assembly, are implemented using DACs to produce analogue control voltages which are sent back to set the photomultiplier EHT levels and log amp limit level respectively. Editorial adjustments, (e.g. original highlight, midtone and shadow) are made digitally in the LUT after the A to D Conversion.

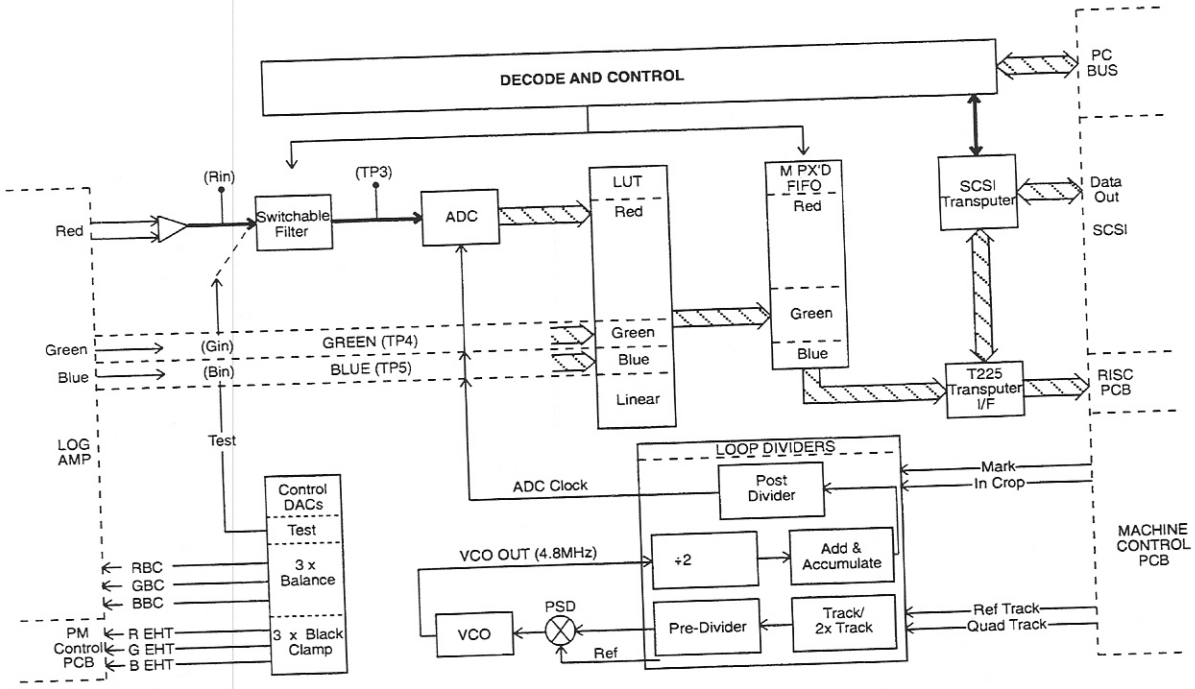


Fig 6.26: ADC PCB Overview

ANALOGUE INPUT BUFFERING AND FILTER

The RGB input signals are sent down three twisted pairs (with each signal paired with the 0v optical unit analogue line) into identical current buffers. Each buffer is low noise, medium speed operational amplifier, connected differentially between the signal and its 0v line. The differential connection removes the effect of differences in signal ground potential between the Log Amp and ADC boards. The 0v lines from the Log Amp are **not** connected back to signal ground on the ADC board.

ADC PCB

An input filter for each channel, reduces the noise bandwidth and signal aliasing into the Analogue to Digital Converter. The filter is a second order Butterworth type with 16 selectable low pass cut-off frequencies (see table 6.4). The cut-off frequency is set by digitally switching in alternate sets of capacitors and resistors using control bits $FC_{1,0}$ and $FR_{2,1,0}$ respectively.

The voltage range from the input filter is scaled in the range of 0V to-5V, therefore an LSB from the ADC corresponds to 1.22mV. The internal reference output from the ADC is used to reference the buffer between the filter and the ADC, to reduce offset error.

Capacitor Selector		Resistor Selector			Cut-Off Frequency (kHz)
FC1	FC0	FR2	FR1	FR0	
1	1	X	X	0	3.5
1	0	X	X	0	5
0	1	X	X	0	7
1	1	0	0	1	10
1	0	0	0	1	14
0	1	0	0	1	20
1	1	0	1	1	28
1	0	0	1	1	40
0	1	1	0	1	57
1	1	1	0	1	80
1	0	1	0	1	113
0	1	1	1	1	167
1	1	1	1	1	225
1	0	1	1	1	320
0	1	1	1	1	450
0	0	1	1	1	900

Table 6.4: Filter Bandwidth Selection

PHOTOMULTIPLIER EHT AND BLACK LEVEL CLAMP DACS

The ADC board provides static analogue control voltages for the Analogue PCBs in the optic assembly. There are three photomultiplier EHT control voltages for balance and three black level clamp (log amp shadow limiting) control voltages. The EHT controls are unipolar, from 0 to -5Volts to the PM Control board and the black clamp drive is bipolar +/-5Volts to the log amp, and are provided by two quad 12 bit DACs.

SELF TEST DAC

There is a provision of a self test signal source on the ADC board for local and overall system testing. An analogue test voltage can be switched into any (or all) of the three analogue channels between the input buffers and analogue filters. The self test DAC is a 12 bit DAC (the fourth section of the EHT control DAC) and a simple analogue change-over switch in each channel is used to switch between the test signal and the input buffer signal. The self test is **not** able to check the differential input buffers.

ANALOGUE CIRCUIT POWER SUPPLIES

To guarantee correct operation of the analogue circuits and maximum immunity from digital signal noise, there are four internally generated power supplies; +10V,-10V,+5Vadc and -5Vadc. The +10V is derived from the PC +12V supply (which is specified in the range 12.6V to 11.4V) and supplies 250mA. The -10V is from the PC -12V supply (which is the range -13.2V to -10.8V). The +/-5Vadc are derived from the PC +12V by a DC/DC converter, rated at 250mA.

ADC CIRCUITS

The ADC used is an AD1671JP, a 12bit multiple subranging converter with an integral track and hold amplifier. The ADC requires a convert pulse between 20ns and 50ns long at a maximum frequency of up to 1.25MHz. The clock frequency is generated by a phase locked loop running at a fixed nominal frequency of 4.8MHz and derived from the drum encoder pulses. A repetitive adder then divides this fixed frequency down to provide the actual sample rate required for the selected input resolution/ enlargement.

The ADC +/-5V supply (200mA for the three channels) is sub-regulated on the board from the raw PC +12V by a TET2421.

Rotate Encoder Connection

The physical connection to the rotate encoder is on the Machine Controller board where the signals are buffered. A 10 way ribbon cable within the PC feeds the encoder signals and INCROP signals required by the ADC board as shown in table 6.5.

PIN	SIGNAL
1	In_Crop
2	0v
3	Mark
4	0V
5	Track A
6	0V
7	Tracl B
8	Spare
9	Rotate Track
10	Gated Mark

Table 6.5: Encoder Cable Connections

The nominal drum speed is between 200rpm and 1500rpm. There are two tracks in quadrature, each giving 1024 pulses per revolution of the drum. The nominal encoder clock frequency is therefore between 5.12kHz and 25.6kHz, however by exclusive-ORing the two pulses and using both edges of the resultant track, an effective frequency range of 10.24kHz to 51.2kHz is available.

ICG

ADC PCB

ADC Clock Phase Locked Loop

The loop divider chip, a composite synchronous timing generator chip (STG), is used in part to provide two stages between the encoder pulses and the phase comparator of the phase locked loop (PLL). The first stage selects either track frequency (F) or double track frequency (2F). The second stage is a three bit programmable pre-divider, which gives an output as near as possible to 5.12kHz, for a given rotate speed. For speeds which are a multiple of 150rpm from 300rpm to 1200rpm the pre-divider output is 5.12kHz, with progressive deviation between, peaking at being at odd multiples of 75rpm. See table 6.6.

Drum Speed [rpm]	Track A Freq [kHz]	Double F Selector	Pre-divisor	Pre-divide O/P [kHz]
300	5.12	Yes	2	5.12
375	6.40	Yes	3	4.27
450	7.68	Yes	3	5.12
525	17.92	Yes	4	4.48
750	12.80	Yes	5	5.12
1000	17.07	Yes	7	4.87
1200	20.48	Yes	8	5.12
1350	23.04	No	5	4.61
1500	25.60	No	5	5.12

Table 6.6: PLL Reference Frequency against Drum Speed and Pre-division

The VCO output frequency is a nominal 4.8 MHz when the input voltage from the phase comparator is 2.5V. In the exceptional case that the loop should come out of lock, an analogue comparator circuit detects if VCO_IN goes below 1.1V or above 3.9V. The lock checking circuit drives a status bit, IN_LOCK, which gives a high level when true. The buffered version of the VCO_IN signal drives the VCO_IN test point.

The loop filter is designed to pass frequencies up to once per drum revolution (up to 25Hz), but rejects the encoder frequency used by the loop, having a 3dB bandwidth of 50Hz and 70dB of rejection at 5kHz.

Clock Adder Accumulator

Once an IN CROP signal is received, an add and accumulate circuit forming part of the loop divider, is used to provide the variable clock frequency needed to give the differing sample rates for the required resolution. The main phase locked loop running at a nominal 4.8 MHz is pre-divided by two to give 2.4MHz. This clocks the 16 bit add and accumulate circuit, and an integer number between 500 and 32767 is added to an accumulator on every clock. The most significant bit from this adder is fed to a programmable 4 bit post divider. The number range from 500 to 32767 gives a programmable fine

adjustment of 64:1, which with a post divide of 10 gives a clock frequency adjustment of 640:1 to guarantee changes in input resolution / enlargement of 0.2%. The maximum conversion frequency is applied to the ADCs is 1.2MHz.

The ADC can be driven from clock pulses from two other sources for test purposes: either from the free-running 5MHz oscillator used for the T225 transputer, or from a transition on the DAC address strobe when writing to the test signal DAC for diagnostic testing. The software can also generate a synthetic 'IN_CROP' signal (to define the start of the 'picture' line).

ADC Modules

The three ADCs are ADC1671 modules. The conversion pulse for the ADC1671 is required to be very short, so that all digital switching is over before the noise sensitive analogue sampling starts. This is achieved by using the signal ENCODE which is common to all three ADCs and is derived as part of the LookUp Table FIFO control state machine.

LOOKUP TABLE (LUT) AND ASSOCIATED OUTPUT FIFO'S

A single look-up table (LUT) is used to modify the data output from the three ADCs to provide the operators "Original Gradation" adjustment.

The LUT consists of three 16Kx4 SRAMs, organised as 12 bits in, 12 bits out with two colour address bits, and is output to multiplexed FIFOs. The LUT is formed into four areas. Three of these are used for the Red, Green and Blue channels. The fourth area is permanently set to give a linear response by mapping addresses directly to data. This facility is included as a quick and convenient method of bypassing the normal colour dependent LUTs, effectively removing the gradation curves from the data path for balancing the PMs etc.

Two programmable devices are used to multiplex the three 12 bits words from the ADCs onto the lower 12 address bits of the LUT SRAMs. A state machine inside one of them (FIFO Control) controls the selection of the ADCs and two most significant address bits of the LUTs. For 12bit operation the data from the LUT is byte multiplexed by two control lines, DATA_LOW and HIGH_SEL, the first set by the PC, the second operating only when multiplexing the second part of a data word which exceeds 8 bits.

Data is shifted via the LUT into the three output FIFOs on each rising edge of their respective Write pulses, R_FFW, G_FFW & B_FFW. The FIFO write strobes are generated, in the correct sequence to enable each ADC word to go through the SRAM LUT and be written into the correct red, green or blue pixel FIFO. At the end of each scan line the false state of the IN_CROP signal resets the FIFOs, clearing away data from the previous line and resetting the accumulator within the clock generator, so that the digitisation is repeatable from line to line.

To load the lookup table, both FIFO CONTROL and the output BYTE MUX are tri-stated, the control line also enable the output of the LUT pointer latches. A pair of data transceivers drive the SRAM data lines.

ADC PCB

T225 TRANSPUTER INTERFACE

A T225 transputer interface is used to pass the RGB data from the FIFO to the RISC Transputer PCB. The data is passed to the Transputer PCB and returned to the ADC for connection to the SCSI link via a 25 way cable.

The T225 transputer external 16bit data bus is connected directly to the FIFO output data bus. The FIFO outputs are tri-stated unless their read strobes are low. Each FIFO is memory mapped in the transputer to a separate 4K of memory space.

A 32Kx8 SRAM external memory is provided to run T225 programs. This memory is only one byte wide and in the top half of the T225 address space. Only the red FIFO status lines are connected to the T225, because all the FIFOs are considered to operate together by the software. The arrangement used allows the T225 to poll the FIFO until a block of 256 pixels are available to be read, to enable it to work on blocks of data and achieve maximum performance.

SCSI INTERFACE TRANSPUTER (TRAM B422)

The B422 Transputer SCSI is used to interface between the RISC transputer and the external Macintosh or OEM controlling computer, is fitted as a daughter board on the ADC PCB. The SCSI external connection is via a short length of ribbon cable connected to a standard 50 way delta connector which goes out through the edge bracket of the ADC board itself.

PC BUS INTERFACE HARDWARE

The ADC PCB card is a simple ISA slave, mapped into the PC I/O space, using a basic hardware interface. The PC interface consists of a programmable address decoder for 32 bytes of the PC I/O address space, currently from 0x340 to 0x35F. It enables the PC to access machine functions such as:-

- Board Identifier, Revision Level, Status and Reset
- Filter Selection
- Test Selection and Voltage DAC
- LUT SRAM Address and Data
- Clock Circuit Loop Dividers
- Photomultiplier HT DACs
- Log amp Black Clamp DACs

The ten PC I/O address lines, SA9 - SA0, along with the PC strobes IOW/ and IOR/ provide the address decoder inputs. The address is decoded in a single programmable device, the three LS PC address lines being buffered and sent around the ADC board as AA2 - AA0. If the address decoded is not in the range relevant to the ADC board these lines are static to reduce the possibility of interference from other bus activity.

The setup data is latched on to the board and to transceivers which are used to buffer the data to and from the PC bus. To minimise noise these data transceivers are only activated when the ADC is being addressed.

A programmable device is used to hold the board identification bytes and buffer the status bits, allowing possible changing of the board's self identification without using links.

SELF TEST AND DIAGNOSTIC OPERATION

Many of the functional units described above are required to work with no drum rotation to run an ADC board self test. There are several levels of self test, the most complete levels are incorporated in the full machine software and run on power up. Lower levels are accessible for diagnosis. *See Section 4 of this manual and fig 4.2.*

The principal elements for self test operation are:

- Select Clock Source:
  - (a) From Drum Encoder as in normal scan mode
  - (b) From a free running 5 MHz oscillator to simulate a scan with drum stationary
  - (c) Clock on DAC load (LDAC/) to single step a data pixel through the board, again with drum stationary.

- Select Channel(s) to be driven by test voltage with the filters normally on maximum bandwidth:
  - (a) Red Channel
  - (b) Green Channel
  - (c) Blue Channel
  - (d) All Channels

- Select Data Output Path:
  - (a) Via the transputer links as in normal scanning
  - (b) Read on to the PC bus from the output of the LUT.

Test DAC Voltage Driving

A test voltage is supplied by the test DAC located as the fourth part of EHT setting DAC. This DAC combined with an inverting buffer, produces a test voltage from 0v to +5V, FFF.

It can be used to generate a ramp which can be used in several ways, depending primarily on the clock mode. In the free running mode this loop will generate a waveform which will give a linear analogue signal ramp, which will be pass through to the data FIFOs.

In single shot mode this ramp is incorporated into a diagnostic test with the input data supplied from the terminal to set the effective DC level. The PC can read the data from the LUT, as described above, and compare data read to data written.

ICG

ADC PCB

SIGNAL MNEMONICS

Mnemonic	Meaning
AA	Buffered Address
ADCCK	ADC Clock
AEN	Access Enable
BCLK	Bus Clock
BCSEL	Black Clamp Select
CAPSEL	Capacitor Select
CONTWR	Control Write
D	Data
EF	Empty FIFO
FC	Filter Capacitor
FD	FIFO Data
FF	Full FIFO
FR	Filter Resistor
HF	Half-Full FIFO
IOR	I/O Read
IOW	I/O Write
LD	LUT Data
LDAC	Load DAC
LUTA	LUT Address
LUTADDWR	LUT Address Write
LUTBFOE	LUT Buffer Output Enable
LUTPTROE	LUT Pointer Output Enable
LUTQ4	LUT Fourth Quarter
LUTTOPC	LUT To PC
LUTWR	LUT Write
PROCLK	Processor Clock
QUADTRACK	Quadrature Track
RBC/GBC/BBC	Red/Green/Blue Black Clamp
RDAC	Read DAC
RDD/GRD/BLD	Red/Green/Blue Data
RDFFR/GDFFR/BLFFR	Red/Green/Blue FIFO Write
RDFFW/GRFFW/BLFFW	Red/Green/Blue FIFO Write
REHT/GEHT/BEHT	Red/Green/Blue EHT control
REFTRACK	Reference Track
RESSEL	Resistor Select
ROP/GOP/BOP	Red/Green/Blue Output
RTEST/GTEST/BTEST	Red/Green/Blue Test
SA	PC Bus Address
SD	PC Bus Data
STATOE	Status Output Enable
T2SELECT	Track Times Two Select
VCO	Voltage Controlled Oscillator
VTEST	Test Voltage
WBSEL	White Balance Select

TEST POINTS

RIN	Red channel Analogue input from line receiver (-0.25V to -4.75V)
GIN	Green channel Analogue input from line receiver (-0.25V to -4.75V)
BIN	Blue channel Analogue input from line receiver (-0.25V to -4.75V)
TP1	VCOIN
TP2	ENCODE
TP3(R)	Red Channel Analogue ADC Input (-4.5V to +4.5V)
TP4(G)	Green Channel Analogue ADC Input (-4.5V to +4.5V)
TP5(B)	Blue Channel Analogue ADC Input (-4.5V to +4.5V)
TP25	Red FIFO Read
TP26	Red FIFO Write
TP27	Green FIFO Read
TP28	Green FIFO Write
TP29	Blue FIFO Read
TP30	Blue FIFO Write
TP31	Full FIFO
TP32	Empty FIFO
TP33	Half-Full FIFO

SCSI CONNECTOR (AD6) PINOUTS

Pin	Signal	Pin	Signal
1	Ground	2	_DB0
3	Ground	4	_DB1
5	Ground	6	_DB2
7	Ground	8	_DB3
9	Ground	10	_DB4
11	Ground	12	_DB5
13	Ground	14	_DB6
15	Ground	16	_DB7
17	Ground	18	_DBP
19	Ground	20	Ground
21	Ground	22	Ground
23	Ground	24	Ground
25	-	26	TERMPWR
27	Ground	28	Ground
29	Ground	30	Ground
31	Ground	32	_ATN
33	Ground	34	Ground
35	Ground	36	_BSY
37	Ground	38	_ACK
39	Ground	40	_RST
41	Ground	42	_MSG
43	Ground	44	_SEL
45	Ground	46	_C/D
47	Ground	48	_REQ
49	Ground	50	_I/O

ADC PCB

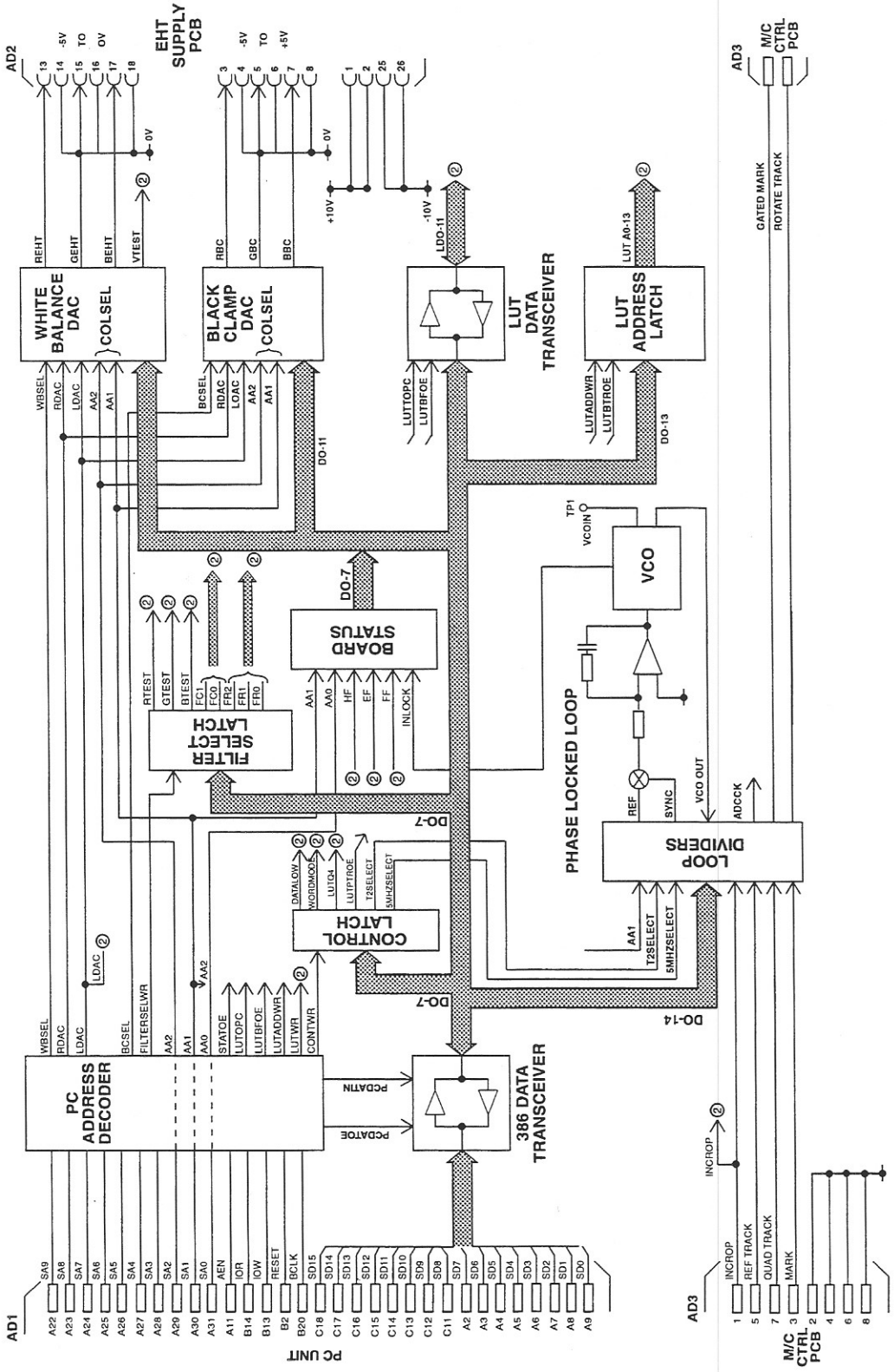
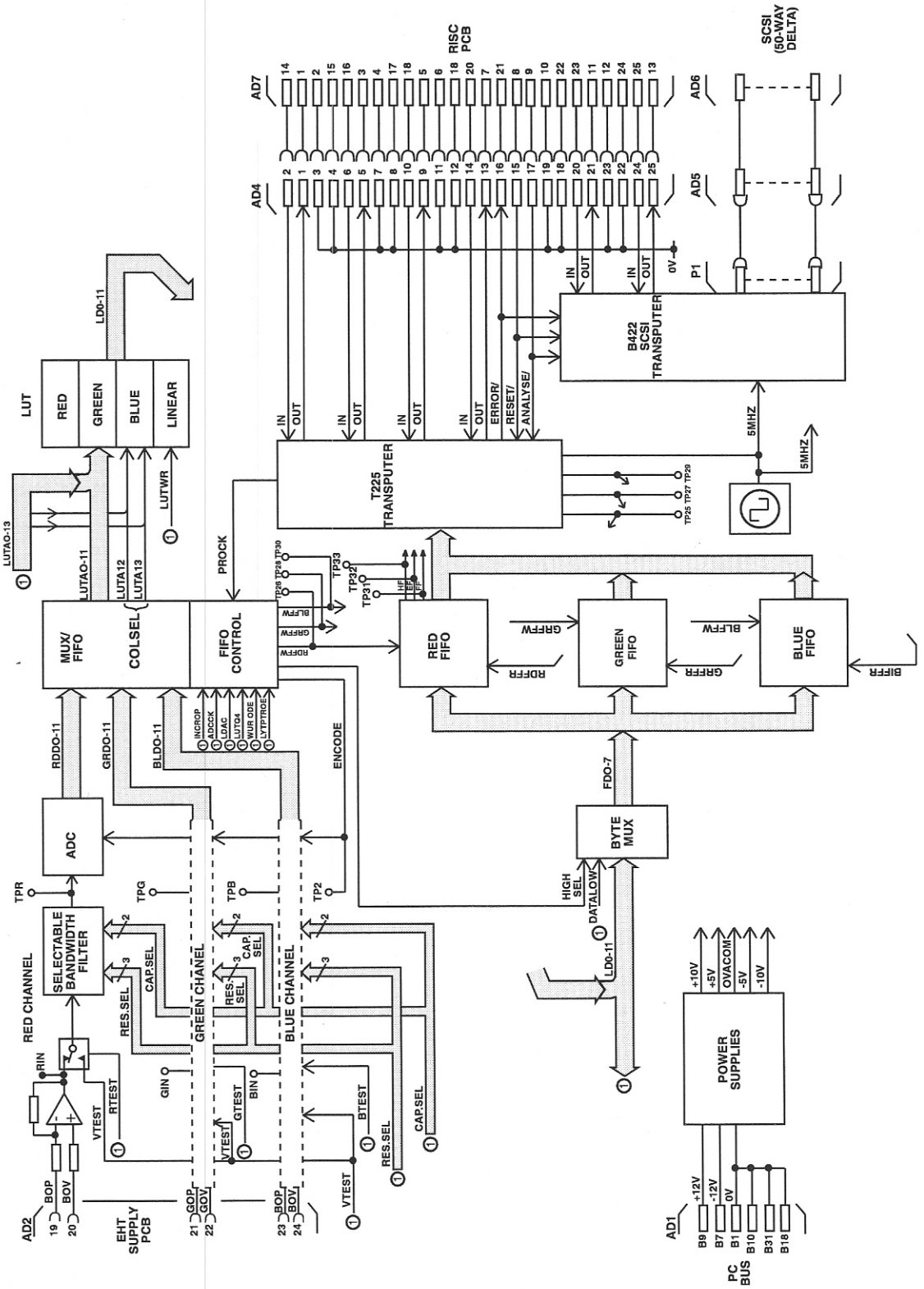


Fig 6.27(a): ADC Board 3500207 (Sheet 1)

ADC PCB


RISC PCB
SCSI (50-WAY DELTA)
AD7
AD6
AD5
AD4
P1
0V
IN
OUT
B422 SCSI TRANSPUTER
T225 TRANSPUTER
ERROR/
RESET/
ANALYSE/
5MHZ
TP25 TP27 TP29
LUT
RED
GREEN
BLUE
LINEAR
LD0-11
LUTWR
LUTAO-13
LUTAO-11
LUTA12
LUTA13
PROCK
TP28 TP28 TP30
TP33
TP32
TP31
HF
EF
PF
MUX/ FIFO
COLSEL
FIFO CONTROL
BLFFW
GRFFW
RDFFW
RED FIFO
GREEN FIFO
BLUE FIFO
RDFFR
GRFFR
BLFFR
INCROP
ADCCK
LDAC
LUT04
WUR ODE
LYTPTROE
RDDO-11
GRDO-11
BLDO-11
ENCODE
FDO-7
ADC
BYTE MUX
HIGH SEL
DATALOW
TPR
TPG
TPB
TP2
SELECTABLE BANDWIDTH FILTER
RED CHANNEL
GREEN CHANEL
BLUE CHANNEL
CAP.SEL
RES.SEL
RIN
GIN
BIN
VTEST
RTEST
GTEST
BTEST
AD2
BOP
BOV
GOP
GOV
EHT SUPPLY PCB
+10V
+5V
OVACOM
-5V
-10V
POWER SUPPLIES
AD1
+12V
-12V
0V
PC BUS

ADC PCB